IDEC Chip Design Contest

The Design of a Low Power Embedded AI System

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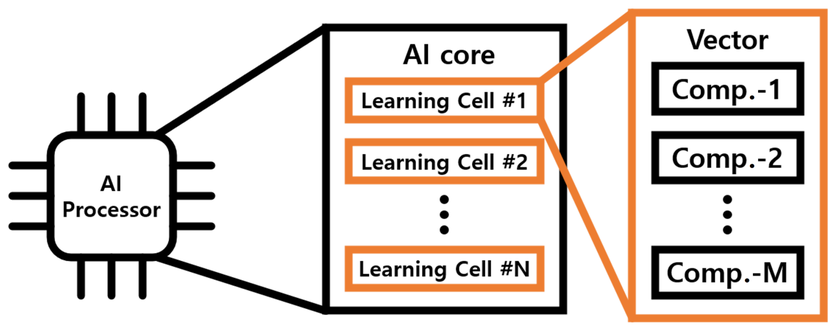
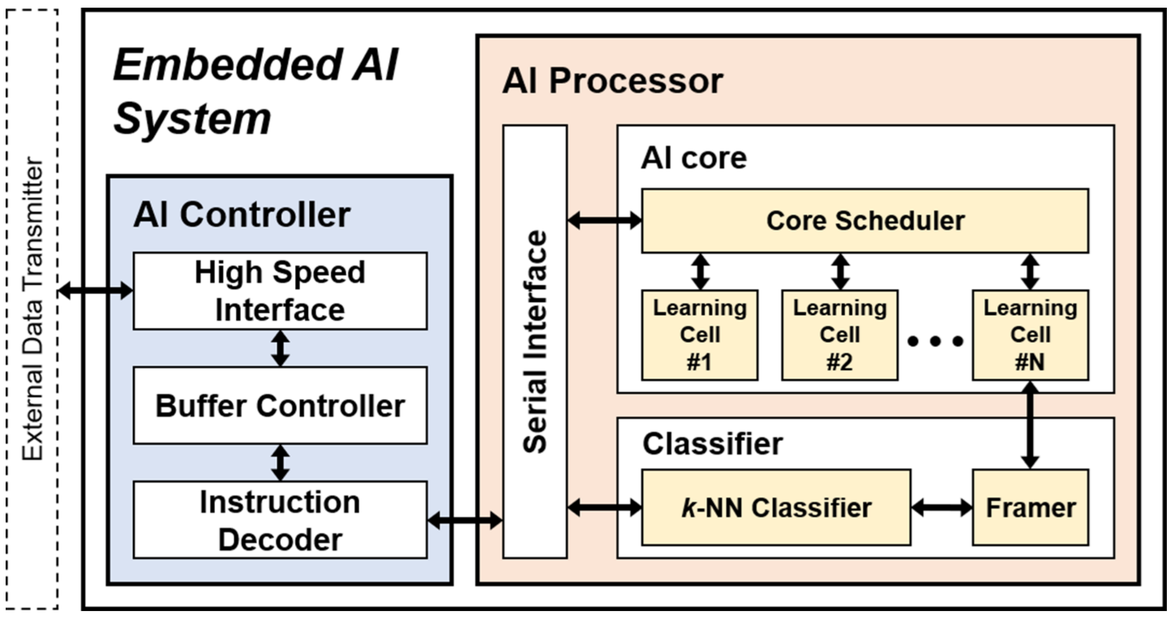
Abstract

We developed a low-power embedded AI system that utilizes the *k*-Nearest Neighbor (*k*-NN) algorithm. The system is designed with an efficient finite state machine controller that has been optimized to generate concise instructions. This design enables the embedded AI system to rapidly train datasets and classify test data with low power consumption. We fabricated the embedded AI system using Samsung's 28nm RFCMOS technology.



[Composition of AI processor]

Architecture



[Architecture of the embedded AI system]

7	6	5	4	3	2	1	0
RW SEL	WRITE MODE		REG				

[7] RW SEL
0: Write
1: Read

[6:5] WRITE MODE
00: Write one
01: Write COMP
10: Write LCOMP
11: Write CAT

[4:0] REG
Address to read or write

※ Data length (L) : Min 1 ~ Max 255

[8-bit setup value]

- **AI Controller**
  - **Buffer Controller:** Stores and transmits instructions and data to the instruction decoder.
  - **Instruction Decoder:** Transmits control data to the AI processor.
- **AI Processor**
  - **Core Scheduler:** Sends the dataset to the learning cell.
  - **Learning Cell:** Each learning cell calculates the distance between the training and test dataset in parallel.
  - **Classifier:** Organizes the distance and category results from each cell.

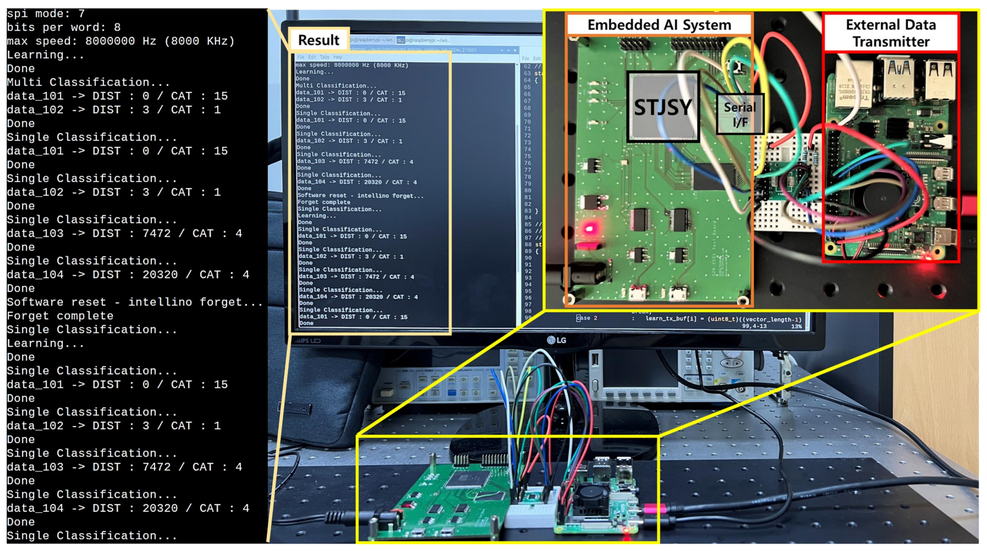
Chip Verification

- **Experimental Environment**

Experimental environment consists of an external data transmitter for transferring the dataset, a prototype PCB including the STJSY, and a serial port.

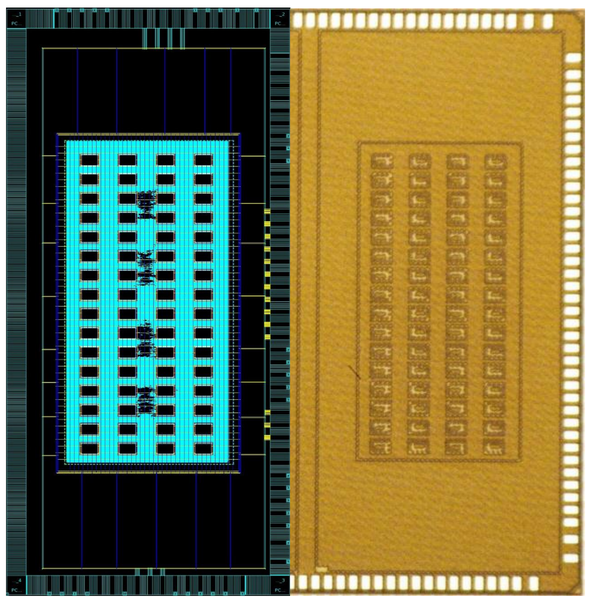
- **Experimental Result**

The proposed system prints '0' as the distance when the system receives the same test data as one of the trained datasets. Additionally, the category of the recognition result is correctly shown. The outputs demonstrate that the system is functioning properly.



[Experimental environment]

Chip Implementation



[Chip layout and photograph]

Chip Specification	
Technology	28nm RFCMOS
Core Voltage	1.0V
I/O Voltage	1.8V
Chip Size	4mmx2mm
Clock Frequency	50MHz
Area	398,058μm^2
Power Consumption	76.03mW
Operating Temperature	-40°C~125°C

Acknowledgment

The chip fabrication and EDA tool were supported by the IC Design Education Center (IDEC), Korea.